AMENDMENTS TO THE SPECIFICATION

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please replace the paragraph beginning on page 9, line 10 with the following paragraph:

B1

The circuit 100 has been described in the context of the example of two delay elements. However, a number of delay elements may be implemented accordingly to meet the design criteria of a particular implementation. For example, a plurality of delay elements 109a-109n may be implemented to provide a variety of programmable delay times for the signal DIN_DLY. In general, particular design parameters may dictate that a fast or a slow delay time of the signal DIN_DLY may be required. For example, one of the delay elements 109a-109n may be appropriate to provide timing that may be used with a circuit such as the circuit 10 of FIG. 1. Furthermore, another one of the delay elements 109a-109n may provide a delay of the signal ~~DLY~~ DIN_DLY appropriate with a circuit such as the circuit 20 of FIG. 2. Furthermore, another of the delay elements 109a-109n may be programmed to provide a delay appropriate for another design application. When the number of delay elements is greater than two, the signal S_H may be implemented as a multi-bit signal. In one example, the signal S_H may be received from an external pin. However, the signal S_H may

B1 end

be received from other sources, such as an internal register, control interface, software instructions, a microprocessor, etc.

Please replace the paragraph beginning on page 4, line 14 with the following paragraph:

B2

The delay circuit 101 may have an input 103 that may receive a signal (e.g., S_H), an input 104 that may receive a signal (e.g., DIN) and an output 105 that may present a signal (e.g., DIN_DLY). The signal DIN_DLY may be presented to an input 106 of the register 102. The register 102 may also have an input 107 that may receive a signal (e.g., CLK). The register 102 may be configured to store the signal DIN_DLY in response to the signal CLK. The register 102 may present a signal (e.g., DOUT). In one example, the signal S_H may be implemented as a setup and hold time configuration signal and the signal DIN_DLY may be implemented as a delayed data signal. In another example, the signal S_H may be implemented as a user configurable signal. For example, the signal S_H may be configured/programmed in a number of ways such as (i) a control interface, (ii) a number of input pins, (iii) software instructions, and/or (iv) hardware. However, the signal S_H and the signal DIN_DLY may be implemented as other appropriate signal types in order to meet the criteria of a particular implementation.